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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,736	06/19/2001	Wilbur G. Catabay	00-654	5658
24319	7590	10/27/2003		
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 LEGAL MILPITAS, CA 95035			EXAMINER	KILDAY, LISA A
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/884,736	CATABAY ET AL.
	Examiner Lisa A Kilday	Art Unit 2829

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(e). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on RCE filed on 9/15/03.
- 2)a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-3 and 22-28 is/are pending in the application.
- 4a) Of the above claim(s) 28 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-3, 22-27 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 - * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) Interview Summary (PTO-413) Paper No(s) _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

Election/Restrictions

Claim 28 withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected specie II, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper filed 9/15/03.

Applicant's election with traverse of specie I in election dated 9/15/03 is acknowledged. The traversal is on the ground(s) that specie I of a single damascene layer is not distinct from specie II of a dual damascene. This is not found persuasive because the applicant admitted that the final products of each specie resulted in different products. Applicant has canceled all claims drawn to a dual damascene and filed a divisional for prosecution of specie II. The applicant has asked to consider figure 6 as part of specie II, dual damascene. Applicant's arguments found persuasive. Figure 6 belongs in specie II because it contains a second densified dielectric layer that is further etched in the dual damascene structure.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1-3, 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (6,028,015). In re claim 1, Wang et al. discloses a process for forming an integrated circuit structure having at least one layer of low k material therein and a

layer, formed from a low k dielectric layer, suitable for use as an etch stop and/or an etch mask which comprises: forming a first layer of low k dielectric material (10) over a previously formed integrated circuit structure (2), and treating the upper surface of said first layer of low k dielectric' material with a plasma to form a first layer of densified dielectric material (14) over the remainder of the underlying first layer of low k dielectric material (fig. 4, col. 2 lines 43-56, col. 3 lines 43-49.), whereby said first layer of densified dielectric material (18) is capable of serving as a etch stop and/or an etch mask (fig. 3, ref. 18) for etching of said underlying first layer of low k dielectric material. However, Wang et al. does not teach forming a first low k material and treating the upper surface of said first low k prior to any exposure of said first low k to etchant. However, selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results *In re Burbans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946). Therefore it would be obvious to one skilled in the art at the time of invention to modify the process of Wang et al. by densifying the first low k prior to etching because densification reduces moisture.

In re claim 2, Wang et al. teaches forming a first photoresist mask (40) with a first pattern of openings (fig. 1) therein over said first layer of densified dielectric material (ref. 14) and patterning said first layer of densified dielectric material through said first openings in said first photoresist mask to form a first etch mask layer of densified dielectric material having a pattern of opening in said first etch mask layer of densified dielectric material suitable for use in etching a corresponding pattern of openings in said underlying first layer of low-k dielectric material (col. 5, line 60- col. 6, line 16).

In re claim 22, Wang et al. teaches removing said photoresist mask (40) from said first etch mask layer of densified dielectric material (18) before etching said first layer of low k dielectric material (col. 3, lines 35-40).

In re claim 3, Wang et al. teaches etching said pattern of opening (12) in said first layer of low k dielectric (10) through said pattern of openings (12) in said first etch mask layer (18) of densified dielectric material thereon.

In re claim 23, Wang et al. teaches a process for forming an integrated circuit structure having at least one layer of low k and a layer formed from said low k, suitable for use as an etch mask which consists essentially of:

- a) Forming a first layer of low k (10) dielectric material over a previously formed IC structure (2)
- b) Treating the upper surface of low k (10) with a plasma formed from a non-oxidizing gas to form a first layer of densified dielectric (14), (fig 4; col. 2, lines 43-56; col. 3, lines 4-49)
- c) Forming a photoresist mask (40) over said first layer of densified dielectric (14)
- d) Patterning said densified dielectric through said photoresist mask to form a first etch mask layer of densified dielectric material having a pattern of openings (12), (col. 5, line 60-col. 6, line 16).
- e) Removing said photoresist mask before etching any openings through said pattern of openings in said first etch mask layer of densified dielectric material (col. 3, lines 35-40);

Whereby the first layer of the densified dielectric material serves as an etch mask (18) for subsequent etching of said underlying first layer of low k. However, Wang et al. does not teach forming a first low k material and treating the upper surface of said first low k prior to any exposure of said first low k to etchant. However, selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results *In re Burbans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946). Therefore it would be obvious to one skilled in the art at the time of invention to modify the process of Wang et al. by densifying the first low k prior to etching because densification reduces moisture.

In re claim 24, Wang et al. teaches the process of claim 23 including the further step of etching said pattern of openings (12) in said first layer of low k dielectric material (10) through said pattern of openings (12) in said first etch mask layer (18) of densified dielectric material thereon.

In re claim 25, Wang et al. teaches the process of claim 24 wherein said pattern of openings (12) etched in said first layer of low k dielectric material (10) through said first etch mask layer (18) comprises a pattern of trenches extending through said first layer of low k dielectric material down to said previously formed integrated circuit structure (col. 1, lines 60-65; col. 2, lines 30-33; col. 4, lines 64-67; col. 5, lines 15-35; fig. 3).

In re claim 26, Wang et al. teaches the process of claim 24 wherein said pattern of openings etched in said first layer of low k dielectric material comprises a pattern of vias extending through said first layer of low k dielectric material down to said previously

formed integrated circuit structure (col. 1, lines 60-65; col. 2, lines 30-33; col. 4, lines 64-67; col. 5, lines 15-35; fig. 3).

Conclusion

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0957. See MPEP 203.08.

Any inquiry concerning this communication from the examiner should be directed to Lisa Kilday whose telephone number is (703) 306-5728. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (703) 308-1233. The fax number for the group is (703) 305-3432. MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

Lisa Kilday

LAK

10/17/03

A handwritten signature in black ink, appearing to read "Lisa Kilday".